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-- This application is a continuation of U.S. Patent Application Serial No. 09/249,388, filed on February 12, 1999, now Patent No. US 6,258,660 B1, which is a divisional of U.S. Patent Application Serial No. 08/940,307, filed on September 30, 1997, both of which are incorporated herein by reference. --

IN THE CLAIMS:

Please amend the claims as follows:

a2 sub B17

1. (Once Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate;

forming an isolation film within said trench, said isolation film having an upper surface;

forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks.

2. (Once Amended) A process of forming a container cell as defined in Claim 1, wherein etching a container cell etches said semiconductor substrate such that a portion of said container cell extends beneath said first gate stack.

8. (Once Amended) A process of forming a container cell as defined in Claim 1, wherein etching a container cell comprises an RIE process.

15. (Once Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate;

forming a conformal isolation film within said trench, said isolation film having an upper surface;

forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film have an interface that extends below said edge into said semiconductor substrate.

16. (Once Amended) A process of forming a container cell as defined in Claim 15, wherein forming an isolation film is performed by forming an oxide film by the decomposition of TEOS.

18. (Once Amended) A process of forming a container cell as defined in Claim 15, wherein etching a container cell comprises an RIE process.

19. (Once Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate by spinning on a photoresist, masking, exposing and patterning said photoresist to create a photoresist mask, and anisotropically etching through said photoresist mask;

forming a conformal isolation film within said trench by forming an oxide film by deposition, said isolation film having an upper surface;

forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said

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container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film form an interface that extends below said container cell into said semiconductor substrate.

20. (Once Amended) A process of forming a container cell as defined in Claim 19, wherein said edge and said interface are coplanar.

21. (Once Amended) A process of forming a container cell as defined in Claim 19, wherein said edge and said interface are not coplanar.

Please add the following new claims:

a6 Sub B3

23. A process of forming a capacitor, comprising:

forming a trench in a semiconductor substrate;

forming an isolation film within said trench, said isolation film having an upper surface;

forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film;

forming a first gate stack upon said semiconductor substrate, said first gate stack having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench;

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks;

forming a storage node within said container cell;

forming a cell dielectric upon said storage node; and

forming a cell plate upon said first gate stack, upon said cell dielectric, and upon said second gate stack.

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24. A process of forming a capacitor, comprising:

forming a trench in a semiconductor substrate;

forming an isolation film within said trench;

forming a first gate stack upon said semiconductor substrate, said first gate stack having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench;

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks;

forming a storage node within said container cell;

forming a cell dielectric upon said storage node; and

forming a cell plate upon said first gate stack, upon said cell dielectric, and upon said second gate stack, wherein said cell plate has an upper surface that extends into said container cell.